

Tutorial for Cadence SimVision Verilog Simulator Tool

T. Manikas and M. Thornton, Southern Methodist University, 6/13/13

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1 Preliminary Setup

Create a separate directory in your account (e.g., SimVision).

2 Creating the Example Verilog File

Make sure that you are in your main separate directory (e.g., SimVision) as mentioned earlier. Using your preferred text editor (e.g., vi, emacs), create a file named **example.v** (note that Verilog files have a *.v extension) and enter the following lines of Verilog code:

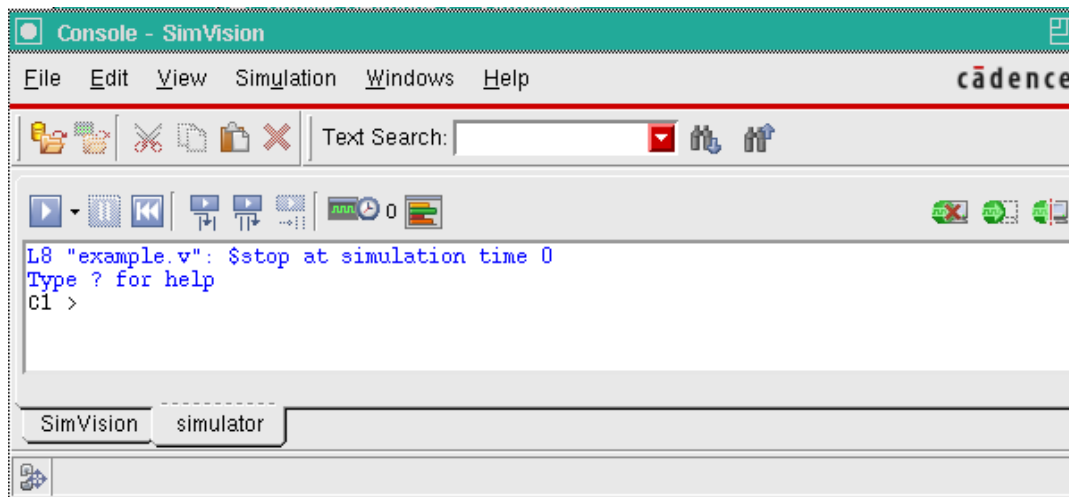
```
// Stimulus for simple circuit
module stimcrct;
reg A, B, C;
wire x, y;
circuit_with_delay cwd (A, B, C, x, y);
initial
begin
  $stop;
  A=1'b0; B=1'b0; C=1'b0;
  #100
  A=1'b1; B=1'b1; C=1'b1;
  #100
  $stop;
end
```

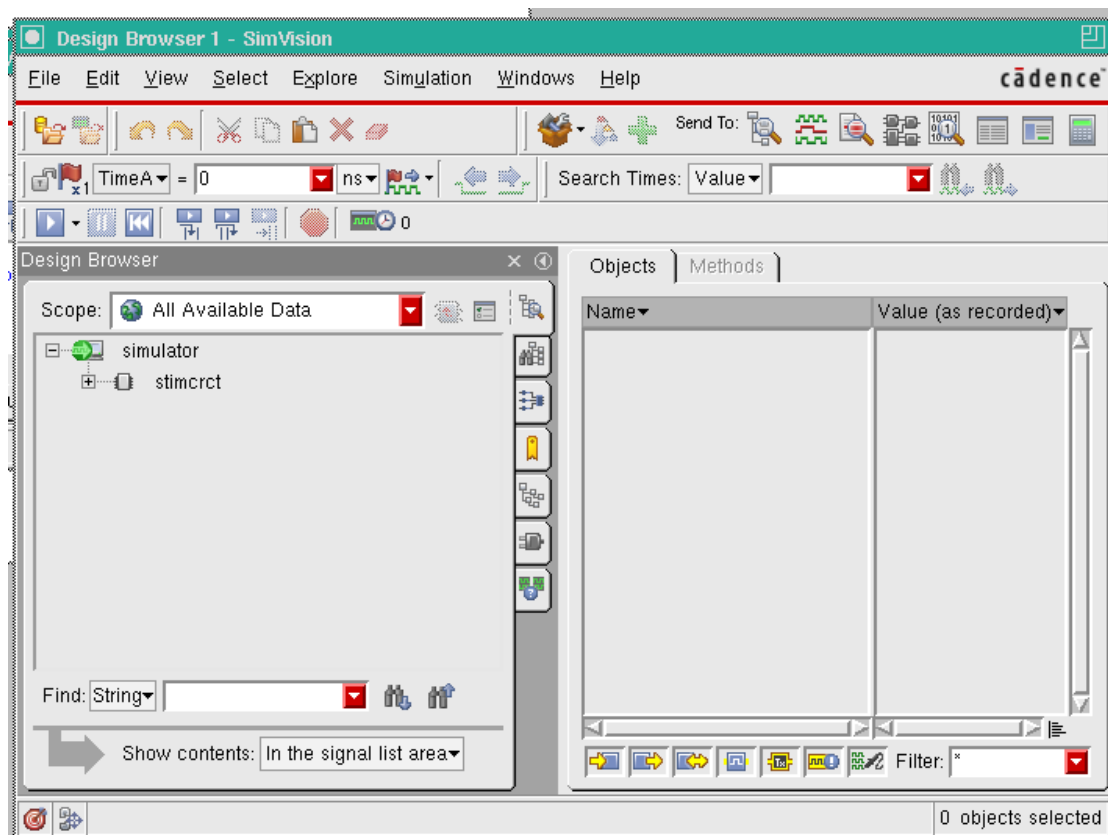
```
endmodule

// Description of circuit with delay
module circuit_with_delay (A,B,C,x,y);
    input A,B,C;
    output x,y;
    wire e;
    and #(30) g1(e,A,B);
    not #(10) g2(y,C);
    or #(20) g3(x,e,y);
endmodule
```

3 Starting SimVision Tool and Reading in the Verilog file

1. Save your Verilog file and exit the text editor.
2. At the Unix prompt, type: **verilog +gui example.v &**
3. If there are no errors, two windows will pop up: **Console** and **Design Browser 1**.
4. However, if there **are** errors, the tool will display the error messages and will not launch these windows. Usually, errors are due to typos in your Verilog file – please correct the errors using your text editor, then try to run SimVision again.

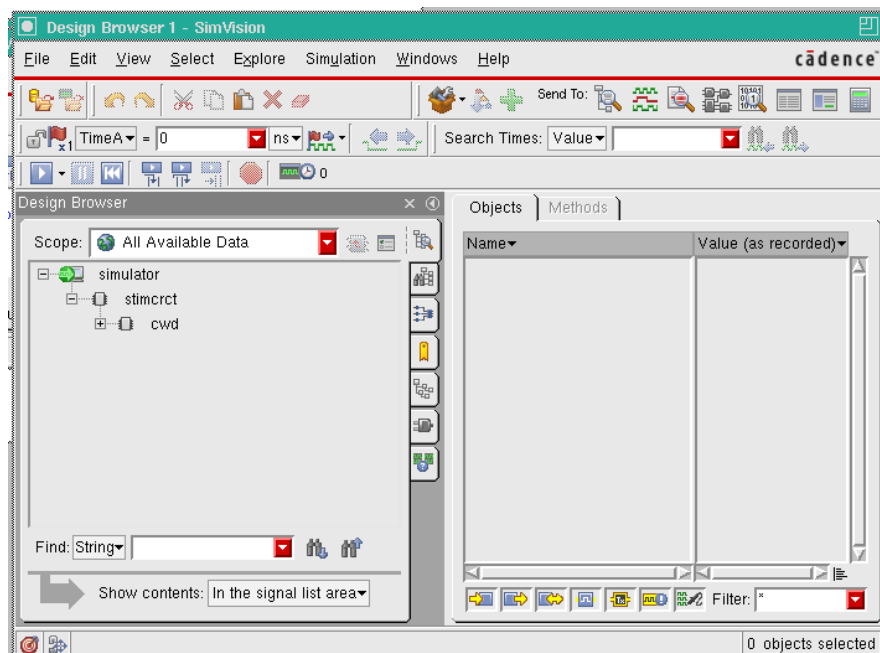




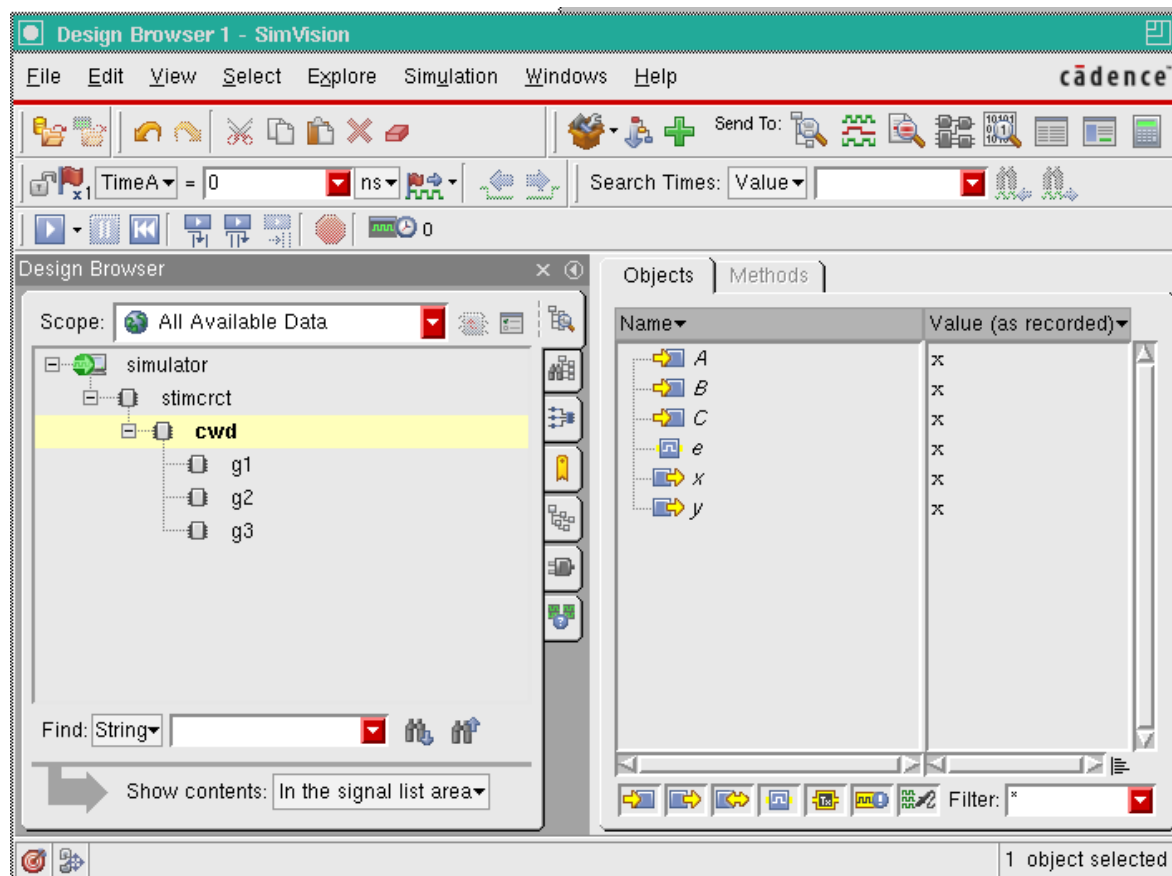
4 View Waveforms

4.1 Setup

1. In the Design Browser Window, click on "+" next to **stimcrct**. This will cause **cwd** to be displayed under **stimcrct**.

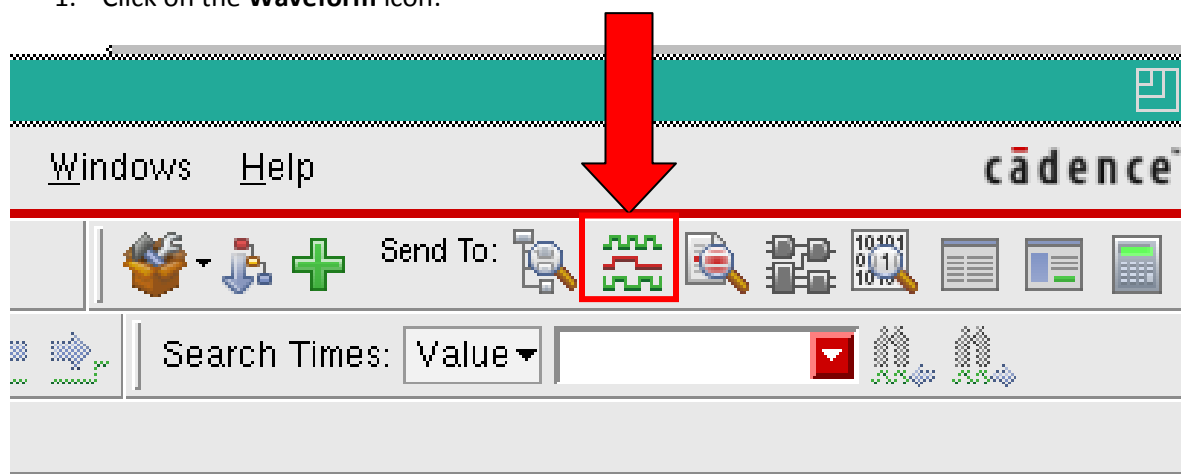


2. Click on "+" next to **cwd**. This will display **g1**, **g2**, and **g3**.
3. Click on **cwd**. This will display all signals (A,B,C,e,x,y) to be displayed in the **Objects** area.

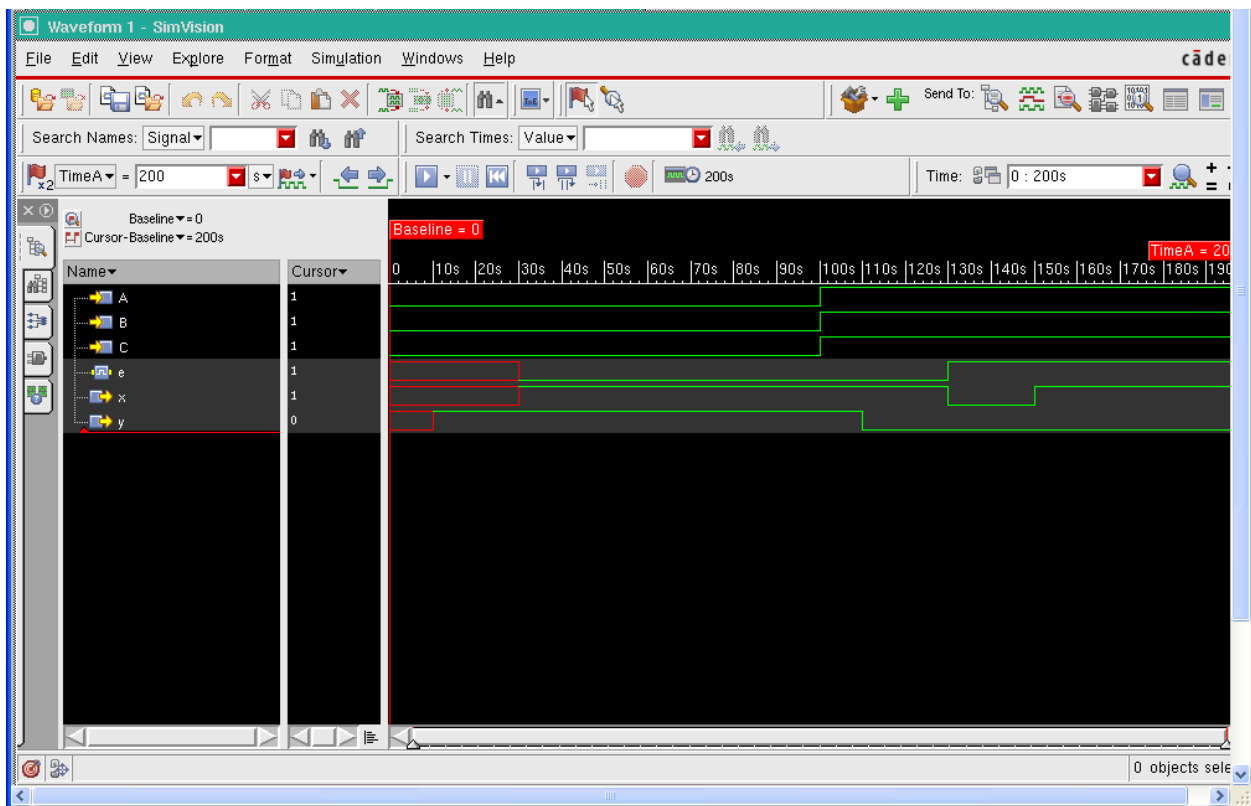
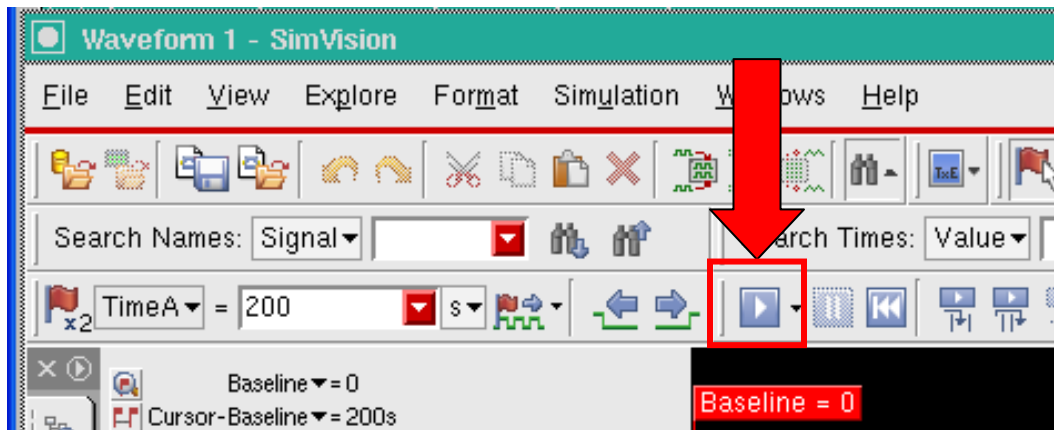


4.2 Waveform Viewer

1. Click on the **Waveform** icon:



2. This will open the **Waveform** window. Click on the **Run** icon to generate the signal waveforms for our example Verilog circuit:

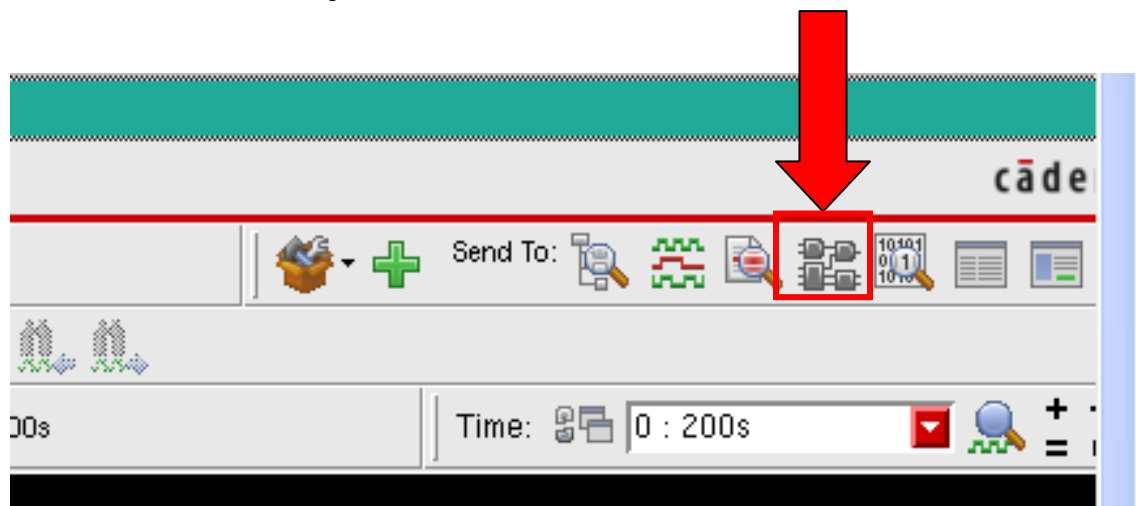


3. Note that output signals **x** and **y** are red lines at the beginning of the simulation. Due to delays through the logic gates, the logic values of signals **x** and **y** are initially undefined.

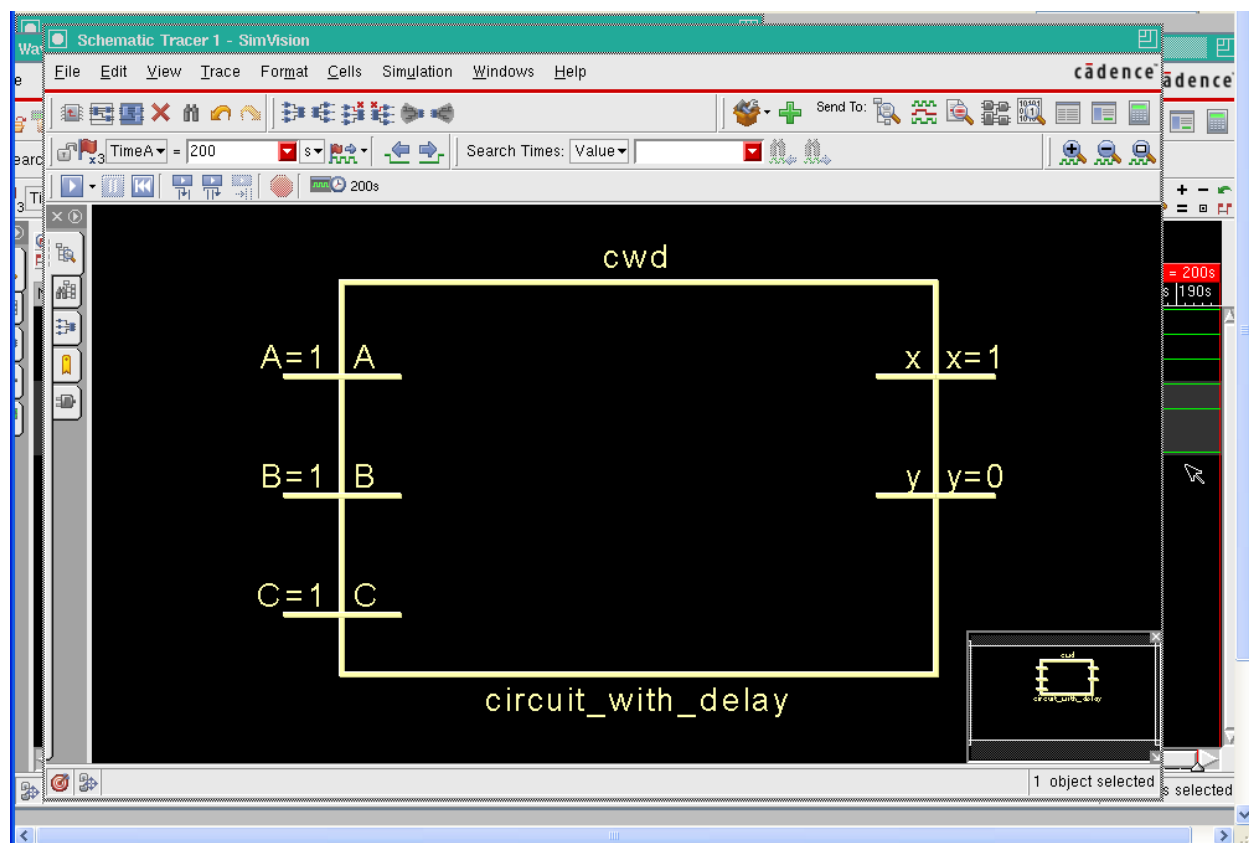
5 Schematic Tracer

Another useful feature of the Cadence SimVision tool is the Schematic Tracer, which displays the corresponding schematic of your Verilog circuit at various levels of hierarchy.

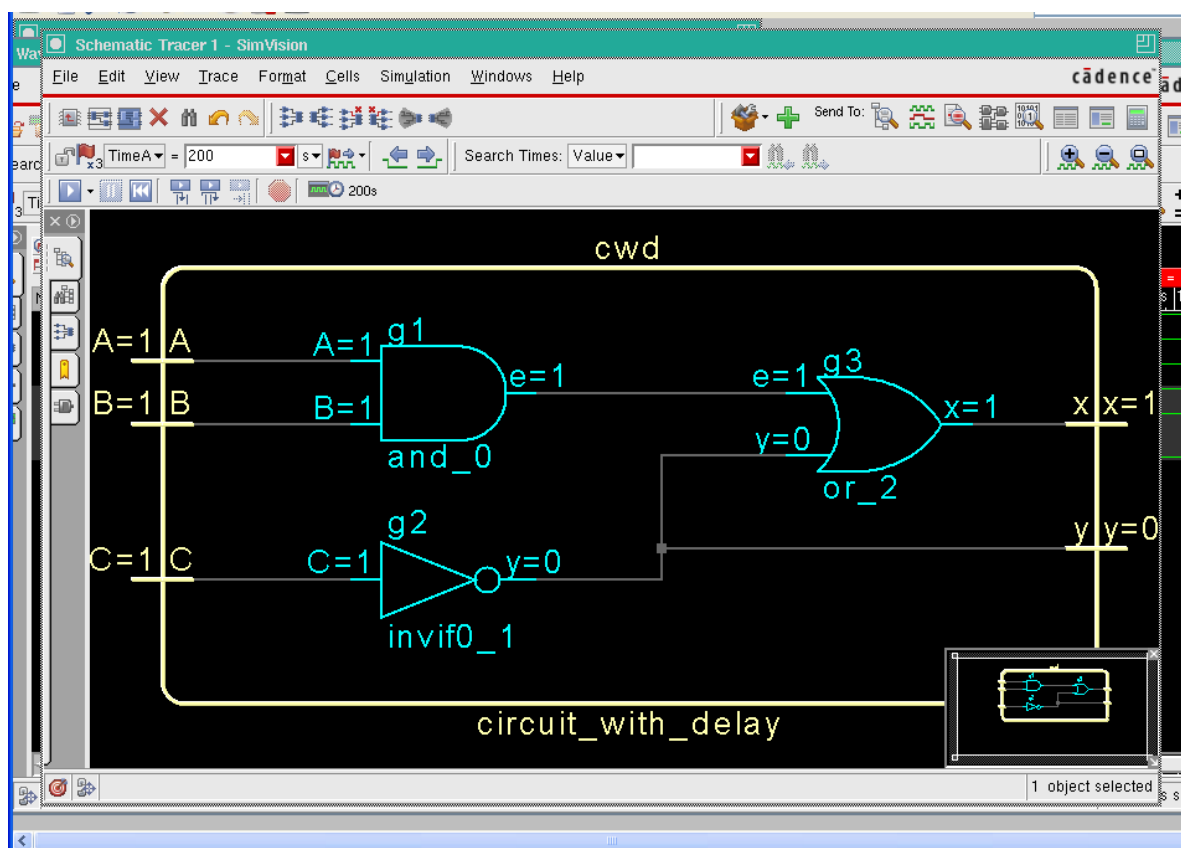
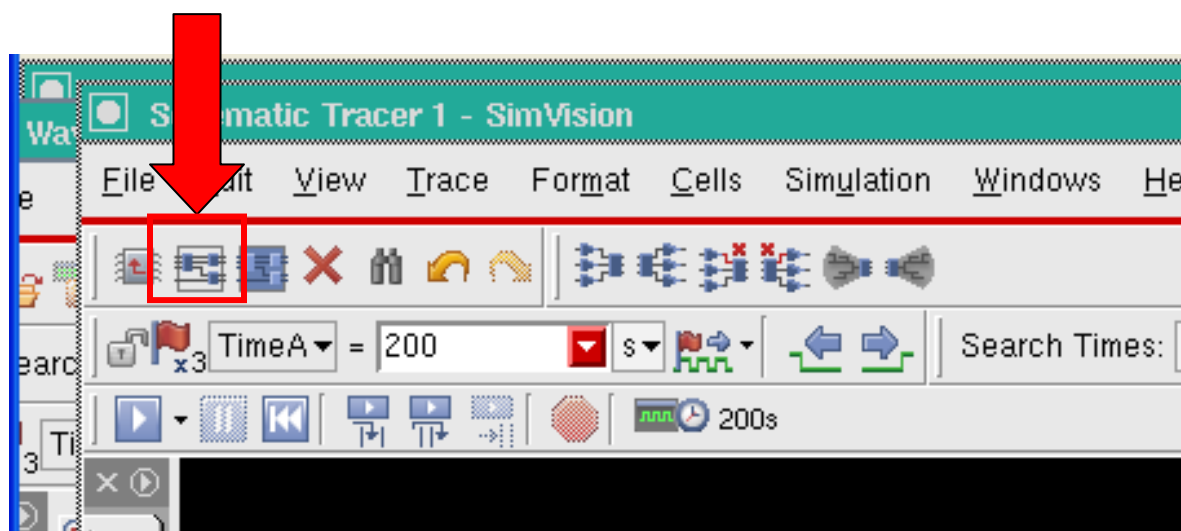
1. In the Waveform window, click on the **Schematic Tracer** icon:



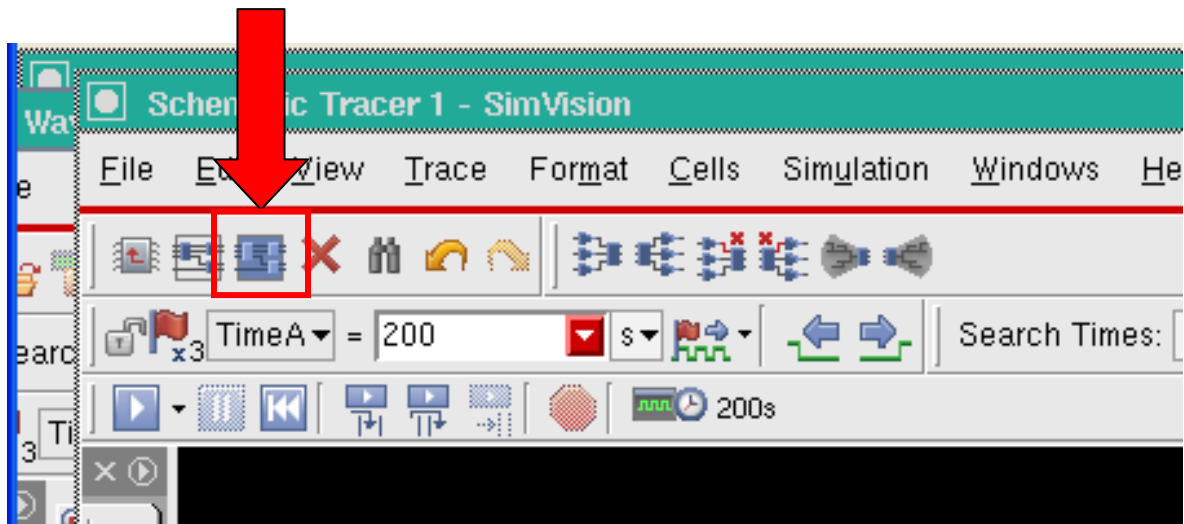
2. This will open the **Schematic Tracer** window and show the instantiation of **cwd**, which is a "black box" representation of our Verilog circuit.



3. To view what is inside the box, click on the **Fill Modules** icon. This will show the logic circuit (logic gates and interconnections) described by our Verilog code.



4. To return to the original "black box" representation, click on the **Collapse Modules** icon:



6 Exiting the Tool

To exit the tool, use the pulldown menu on any of these windows and select **File, Exit SimVision**.