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# Wafer Scale Transfer of Ultra-Thin Silicon Chips on Flexible Substrates for High Performance Bendable Systems

*William Taube Navaraj[1], Shoubhik Gupta[1], Leandro Lorenzelli[2], Ravinder Dahiya[1]**

Ravinder.Dahiya@glasgow.ac.uk

[1]Bendable Electronics and Sensing Technologies (BEST) group, Electronics and Nanoscale Engineering, University of Glasgow, G12 8QQ, United Kingdom
[2]Microsystems Technology Research Unit, Fondazione Bruno Kessler, Trento, 38123, Italy

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This paper presents an innovative approach for wafer scale transfer of ultra-thin silicon chips on flexible substrates. The methodology has been demonstrated with various devices (ultrathin chip resistive samples, MOS capacitors and n-channel MOSFETs) on wafers up to 4" diameter. This is supported by extensive electro-mechanical characterization and theoretical analysis, including finite element simulation, to evaluate the effect of bending and the critical breaking radius of curvature. The ultra-thin chips on polyimide did not break until the radius of curvature of 1.437 mm. In the case of MOS capacitors the measured capacitance increases with increase in bending load. The changes in the transfer and output characteristics of ultra-thin MOSFETs closely match with the theoretical model utilizing empirically determined parameters. Overall, the work demonstrates the efficacy of the new methodology presented here for wafer scale transfer of ultra-thin chips on flexible substrates. The presented research will be useful for obtaining high performance and compact circuits needed in many futuristic flexible electronics applications such as implantable electronics and flexible displays. Further, it will open new avenues for realizing multi-layered multi-material (foil-to-foil) integrated bendable electronics.

## 1. Introduction

Electronic devices and circuits are conventionally fabricated on rigid and flat substrates such as silicon (Si) wafers as current micro/nanofabrication technology allows realizing devices on planar substrates only. Resulting planar electronics has revolutionised our lives enabling fast communication and computing, but the lack of bendability presents challenges for using them in emerging applications such as wearable and implantable electronics, and robotic skin etc. These applications require high-performance electronics to conform to curved surfaces[1]. For this reason, there is a huge interest in obtaining electronics on flexible and non-conventional substrates such as soft plastics and even paper[2]. Smartphones with roll-up displays and healthcare patches attached to the skin to deliver drugs or monitor vital signs etc. are some other areas which will benefit from electronics on flexible substrates[1c, 2b]. The bendability along with high-performance (e.g. fast transistor switching for faster computations and communication) is critical in these emerging applications. As an example, for internet of things (IoT) to be successful, the pivotal enablers such as active Radio Frequency Identification (RFID) tags, communication stack etc. should be able to handle data in ultra-high frequencies (0.3 – 3 GHz) range [3]. Because most of the things in the real world are curvy, these RFIDs should be curvy too and hence both flexibility and high-performance are needed.

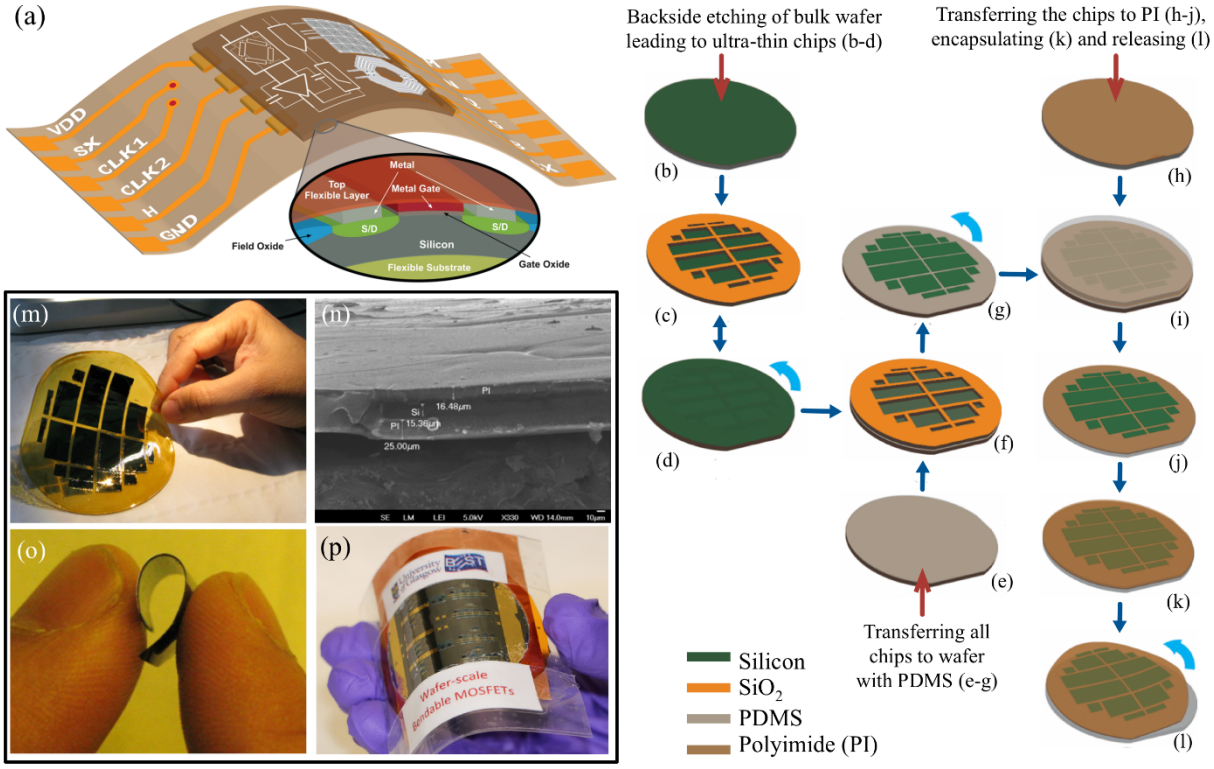


**Figure 1.** a) The scheme of UTCs with integrated multi-materials stack on foil. b-l) The process flow of fabrication and wafer scale transfer of UTCs to flexible polyimide: (b) Initial wafer. (c) the back and, d) front of the wafer after chemical etching. e) A temporary second wafer spin coated with ~ 200 µm thick PDMS. f) The wafer with thin Si chips placed on the second wafer. g) Laser cutting of the top wafer on PDMS to remove the bulk Si, leaving behind the UTCs on the second PDMS coated wafer. h) A third temporary wafer with final substrate (~15µm thick polyimide). i) Bonding of the second wafer (after UTCs transfer) with the third wafer. j) Chemical etching of PDMS to remove the second wafer. k) Spin coating another layer of polyimide to encapsulate the UTCs. l) The final wafer-scale UTCs released from the third wafer; m) Image of the transferred UTCs. n) The cross-sectional SEM image of Si chips encapsulated in polyimide. o) The bending of bare Si chip and, p) MOSFET laminated between PVC sheets.

Tremendous progress in the field of flexible electronics during the last decade has mainly come through organic semiconductors and various printing and stamping techniques[4].

Organic semiconductors have been preferred because of inherent mechanical flexibility and low fabrication costs as they can be printed. However, the modest performance that has thus far been possible with organic devices limits their utility to low-end applications such as passive RFID tags and OLED displays[2a]. This is because of low mobility (~1 $cm^2/V.s$, maximum reported ~43 $cm^2/V.s$[5]) and the technological limitations such as poor resolution of printers (currently best resolution is ~ 20 μm[4e]). The latter is relevant as it defines the channel length ($L$) of a transistor and both the charge carrier mobility ($\mu$) and $L$ affect the transistor transit frequency ($f_T \sim \mu/L^2$) – a measure of the intrinsic speed of a transistor and their performance. The higher charge carrier mobility and shorter channel lengths enhance the speed of transistors[6]. In this regard, the transistors made from materials such as single-crystal Si offer better alternatives for flexible electronics. As an example, on the basis of mobility (~1000 $cm^2/V.s$ for Si cf. ~1 $cm^2/V.s$ for organic semiconductors) alone, a Si based transistor will be 3 orders of magnitude faster than organic semiconductor or a-Si:H based devices[7]. Further, up to 9 orders of magnitude higher performance is achievable if small channel length (<100 nm with micro/nanofabrication cf. >20 μm with printing technologies) of Si devices is considered. Clearly with flexible Si based devices it will be possible to achieve the performance needed for many emerging applications such as IoT, electroceuticals,[8] etc. For this reason, new routes for high-performance flexible electronics have been explored recently with Si. These include using 1-dimensional (1-D) or quasi 1-D Si micro-/nano-structures (e.g. nanowires) based Field Effect Transistors,[9] Light Emitting Diodes,[10] Nano-generators,[11] Solar Energy Conversion Devices,[12] and circuits such as Complementary Inverters,[13] and Image Sensors circuitry. However, the micro-/nanoscale structures based approach is still at infancy for high-performance bendable Integrated Circuits (ICs), which are much needed in many applications such as drive electronics for fully flexible displays, and electronic skin etc. Since ICs on standard Si wafers are known to have better uniformity and stability, the ICs on thinned Si wafers over foil, illustratively shown in **Figure. 1(a)**, will be an attractive route for high-

performance flexible electronics[14]. Towards addressing this need, this work presents a low-cost approach for obtaining ultra-thin chips (UTCs) at wafer-scale and for the first time reports the wafer-scale transfer of UTCs onto flexible substrates.

This paper is organised as follows: The sample fabrication and methodology for wafer thinning and wafer scale transfer of UTCs is presented in **Section 2**. This has been demonstrated with the transfer of various samples obtained with increased fabrication complexity. These include ultra-thin silicon resistive membranes, MOS capacitors (MOSCAP) and n-channel MOSFETs. These devices have been characterized in detail in **Section 3** to evaluate the effectiveness of proposed methodology. The analysis includes finite element modelling, estimation of critical bending, electro-mechanical characterization and bending induced deviations in basic electrical parameters of devices on thin Si. The changes in material properties like transmittance and surface morphology have also been studied to understand the new avenues UTCs offer in terms of applications. Finally, results are summarized in **Section 4**.

## 2. Fabrication and Transfer Methodology

Si wafers start to lose their rigidity when they are thinned down to around 150 μm[15]. Below 50 μm they get more flexible and stable, and below 10 μm the Si membrane starts to become optically transparent[1k]. Using a combination of pre/post-processes steps a few solutions for chip-scale fabrication of UTCs have been reported in literature[15-16]. At wafer scale, the methods that have been explored majorly includes dry etching, mechanical grinding from backside of bulk[1k] as well as SOI[17] wafers and thinning with wet and/or dry etching{Gupta, 2018 #973}. Mechanical grinding is a costly step and there is risk of developing micro-cracks and breakage of wafer during delamination from tape. The SOI wafers based approach is relatively free from the micro-crack issue, but the cost concern remains as the SOI wafers are generally costlier than bulk wafer by an order of magnitude. A few recent methods for UTCs include controlled spalling technique for wafer scale transfer of integrated circuits from SOI wafers[18] or mechanical exfoliation of transistors from bulk wafers[19]. The mechanical

exfoliation process is known to increase the gate leakage current, which degrades the electrical performance of devices. A combination of deep reactive ion etching (DRIE-BOSCH) process and isotropic etching has been used to achieve semi-transparent high performance flexible electronics from bulk Si at an area of 3.75 $cm^2$ (2.5 cm×1.5 cm)[20]. A similar process has been used to realize flexible dies (comprising FinFETs) with an area of 7.5 $cm^2$ (2.5 cm×3 cm)[21]. The cost associated with DRIE and the loss of wafer area because of holes needed for release of the top layer make it difficult to use this process for high density integrated circuits. In Table 1, we have summarized some state-of-the-art works, which uses the various techniques mentioned above to achieve UTCs in a chip scale or wafer scale.

**Table 1. Various works realizing ultra-thin silicon using dry etch, wet etch, grinding and exfoliation**

| Work | Initial Si Wafer | Wafer Scale | Method | Devices | Ref. |
|---|---|---|---|---|---|
| G.A.T. Sevilla *et al.* | SOI | No | Dry Etch | FinFETs | [22] |
| A. Vilouras *et al.* | Bulk | No | Grinding | MOSFETs, Inverters | [23] |
| G.T. Hwang *et al.* | SOI | No | Wet Etch | RFICs | [24] |
| Y. Zhai *et al.* | Bulk | No | Exfoliation | MOSFETs | [25] |
| J.P. Rojas *et al.* | Bulk | No | Dry Etch | FinFETs | [26] |
| A. Diab *et al.* | SOI | No | Dry Etch | FinFETs | [27] |
| H.C. Ko *et al.* | SOI | No | Wet Etch | Photodetectors | [28] |
| M.T. Ghoneim *et al.* | Bulk | Yes | Dry Etch | Ferroelectric Memory | [29] |
| D. Shehrjerdi *et al.* | SOI | Yes | Exfoliation | MOSFETs, Inverters | [30] |
| G.A.T. Sevilla *et al.* | Bulk | Yes | Dry Etch | MOSFETs, Inverters | [31] |
| This work | Bulk | Yes | Wet Etch | Resistors, MOSCAPs, MOSFETs | |

Compared to these methods, wet etching is relatively less costly and free from the issues of micro-cracks. Since the active layer remains unaffected during backside etching, there is no adverse impact on device response after etching. The method presented in this paper is based on the chemical thinning of wafers down to ~15 μm and then transferring the UTCs to flexible polyimide[1b, 32]. The transfer printing that has thus far been used to transfer quasi 1-D micro/nanostructures such as nanowires or ribbons to flexible substrates has been extended here for the first time to achieve wafer-scale transfer of UTCs[1b, 4f, 32]. The post-processing steps shown in **Figure. 1(c-l)** follow the fabrication of devices on the top of silicon.

4" p-type, double side polished Si wafers (resistivity 10-20 $\Omega - cm$) were used in this study. Initially the ultra-thin resistive structures were fabricated and transfer printed. The pre-processing step used for achieving the UTC involves thermal growth of $SiO_2$ on the rear side of the wafer and patterning it to act as hard mask for chemical etching during post-processing as shown in **Figure. 1(c-d)**. UTCs of various sizes (0.5 cm x 0.5 cm; 0.5 cm x 1.5 cm; 2.0 cm x 1.5 cm; and 3.5 cm x 1.5 cm) were obtained by BOE etching of photolithography defined patterns on rear side. The defined patterns considered the dimensional corrections needed due to anisotropic etching with TMAH. The resistive elements were realized from phosphorus doped ($\sim 10^{16}/cm^3$) wafers. The doping, achieved through ion-implantation on the front side, led to a shallow n-junction of ~0.5 μm depth. Then the wafers with resistive elements were carefully mounted on a teflon jig with a double O-ring system to seal the devices on the front side from getting attacked by the etching chemical, while the rear side is open for the chemical to etch. After this, the chemical etching of the wafer was carried out using 25 wt% TMAH (Tetra-methyl-ammonium Hydroxide) solution. The etching was performed until the thickness of wafer reached around 15 μm. At this stage, the thinned portion of wafer can be termed as silicon membranes. During the etching process the thickness of wafer was monitored using profilometer and ex-situ inspection. In principle, etching for longer time could further reduce the thickness of Si membranes. However, due to thickness tolerance related variations in the wafers it is challenging to obtain Si membranes with thicknesses below 10 μm. The jig was carefully raised from the TMAH solution once the etching is complete. The doping controlled etching could be exploited to control the thickness of the membranes. As an alternative, SOI wafers could also be used to obtain thinner membranes as the etching process will be stopped by the buried oxide, which is typically 2-3 μm below the top surface.

After chemical etching, the transfer of UTCs on to flexible PI substrate was carried out following the steps shown in **Figure. 1(e-l).** With front side down the membranes were adhered to a carrier substrate which is a ~200 μm thick PDMS (Poly dimethyl siloxane) spin coated on

another temporary wafer. The adhesion of membranes with PDMS was controlled by a low power plasma. The wafer was then diced around the thinned regions and the bulk Si was removed, leaving behind the Si membranes on PDMS. This wafer-scale transfer step results in the front-sides of UTCs facing towards PDMS. To gain access to the front side, the membranes were transferred once again to the final receiving substrate i.e. polyimide foils. The polyimide foil was obtained by spin coating PI2611 (from HD Microsystems) on a temporary glass wafer and curing it for 30 minutes at 350°C. The glass wafer was used here because of polyimide's poor adhesion with glass, which allows easy release of foils after the transfer process is completed. An adhesion promoter (VM652 from HD Microsystems) was used at the edges of the wafer to temporarily hold the polyimide on glass wafer[15, 33]. Another thin polyimide layer, spin coated on top of cured polyimide foil, acted as adhesive during the transfer of UTCs from PDMS to polyimide. The polyimide is used in this work as the final substrate due to excellent features such as high glass transition temperature and good thermal and dimensional stability. These features enable a finer interconnection pitch, better reliability and compatibility with existing semiconductor technology. The PI2611 has the coefficient of thermal expansion (CTE) of 3 ppm/°C, which matches that of Si (3.2 ppm/°C). This matching of thermal coefficients prevents thermal stress build up in the UTCs during curing of polyimide as well as any residual bending thereafter. The temporary wafer having membranes on PDMS was then placed on polyimide film and soft baked in vacuum at 110°C for one minute, leaving the membranes sandwiched between polyimide and PDMS. Following this the PDMS was removed by dissolving it in a dilute solution of Tetra Butyl Ammonium Fluoride (TBAF) in a hydrophobic non-hydroxylic aprotic solvent such as Propylene Glycol Methylether Acetate (PMA)[34]. This completes the wafer-scale transfer of UTCs on polyimide. The UTCs can be encapsulated by spin coating another polyimide layer on the top of transferred UTCs or using hot lamination method. This process was followed to obtain various devices (**Table 2**) including MOSCAPs and n-channel MOSFETs. As an alternative to above process, a Si wafer with thermally grown

$SiO_2$ on the front side can also be used as the second temporary wafer. The latter two temporary wafers could be mechanical grade as they are used for transfer only. For the same reason, they could be reused to improve the cost effectiveness of the process. Even when considering all 3 wafers as prime grade and assuming all are consumed in one transfer process the total cost will be ~$150 (considering the typical cost of a 6-inch prime grade Si wafer is ~$50). However, if the two-temporary wafers are mechanical grade (cost ~$20/wafer), this total cost will come down to ~$90. If we reuse the temporary wafer (as proposed here) then the cost will further reduce to ~$50. This is much lower than the typical cost of SOI wafer (~$1000 per 6-inch wafer) used in some other approaches referenced in Table1.

**Table 2. Various samples used for bending, optical and electrical analysis with their key specifications**

| Sample ID. | Structure | Width [cm] | Length [cm] | Si Thick -ness [μm] | Key Parameters |
|---|---|---|---|---|---|
| RBC1 | Si membrane with free ends | 1.5 | 0.5 | ~15 | **Critical theoretical ($R_{BC}$):** 1.097 mm<br>**$R_{BC}$ (Expt.) :** <1.1 mm |
| RBC2 | Si membrane with two ends anchored using conductive paste | 1.5 | 0.5 | ~15 | **Critical theoretical ($R_{BC}$):** 1.097 mm**$R_{BC}$ (Expt.) :** <1.19 mm |
| RBC3 | Si membrane encapsulated in polyimide and the two ends anchored using conductive paste | 2.0 | 1.5 | ~15 | Transferred to 25 μm thick polyimide (PI) and encapsulated with 16.48 μm thick polyimide on top<br>**Critical theoretical ($R_{BC}$):** 1.1428 mm with 25 μm/15.36 μm/16.48 μm $PI_{Top}$/Si/$PI_{Bot}$ concave up and 1.437 mm when concave down<br>**$R_{BC}$ (Expt.) :**<1.475 mm |
| UVN1 | Thin Silicon | 2.0 | 2.0 | 15 | Net Vis. Transmittance (390 to 700nm) %: 0.170<br>Net Transmittance (300 to 1100nm) %: 8.694 |
| UVN2 | Thin Silicon | 2.0 | 2.0 | 30 | Net Vis. Transmittance (390 to 700nm) %: 0.011<br>Net Transmittance (300 to 1100nm) %: 8.380 |
| UVN3 | Thin Silicon | 2.0 | 2.0 | 75 | Net Vis. Transmittance (390 to 700nm) %: 0.000<br>Net Transmittance (300 to 1100nm) %: 6.090 |
| UVN4 | Bulk Silicon | 5.1 φ* | - | 300 | Net Vis. Transmittance (390 to 700nm) %: 0.000<br>Net Transmittance (300 to 1100nm) %: 0.927 |
| MOSCAP | MOS Capacitors on p-Si (Wafer scale transfer to polyimide and laminated with PVC) | 5.1 φ* | - | ~15 | Specifications - Au/Ni 100 nm/10 nm as Gate; Oxide Thickness: 100 nm; Si Thickness: ~15 μm; Channel Length x Width: 10 μm x 100 μm; Al 100 nm back metal; Area 0.48 $cm^2$; Encapsulated with 100 μm PVC lamination with Cu backing |
| MOSFETs | n-MOSFETs on wafers (Wafer scale transfer to polyimide and laminated with PVC) | 5.1 φ* | - | ~15 | Specifications - Au/Ni 100 nm/10 nm; Oxide thickness: 100 nm; Si thickness: ~15 μm; Channel Length x Width: 10 μm x 100 μm; Al 100 nm back metal; Encapsulated with 100 μm PVC lamination with Cu backing;<br>**Saturation Mobility:** Zero Bending: 350 $cm^2$/V-s; Tensile Bending: 384 $cm^2$/V-s; Compressive Bending: 333 $cm^2$/V-s |

***** Indicates Diameter

The MOSCAPs and MOSFETs were fabricated on 2" p-type 1-10 Ohm-cm, <100> Si wafers. For MOSCAP, 100 nm thick high quality silicon dioxide was grown via dry oxidation at 1000°C. Nickel (10 nm) and gold (100 nm) were evaporated by electron beam evaporation system and patterned to define the top electrode. A single MOSCAP has an area of 0.48 $cm^2$. For MOSFETs we have used 5 mask process which is schematically summarised in **Figure. 2 (b1-b8)**. A field oxide of ~0.5 μm was grown on the top of the wafer which was later used to isolate diodes of adjacent MOSFET as well as a hard mask in the rear to protect support boundaries during latter thinning. Lithography was carried out after patterned oxide layer in the front side and the

exposed area was etched. Phosphorus was then diffused at 970˚C for 30 minutes through the opened window for creating source and drain region of the transistor as illustrated in **Figure. 2(b2)** targeting a junction depth of ~0.5 μm with measured sheet resistance of ~7.4 Ω/□. After defining the active region, a high quality thin oxide of ~100 nm was grown. The contacts holes for diodes were opened through gate oxide itself and metal stack of Ni/Au (10 nm/100 nm) was evaporated. In last stage of fabrication, metal was patterned to define the contact pads and interconnection, and sintered in forming gas at 450°C to get better ohmic contact. The gate length was of 10 μm (with further 5 μm overlap on each diode regions) and channel width of 100 μm. The front sides of wafer were protected from etchant (i.e. TMAH) by ProTEK B3 protective coating from Brewer Science and a custom wafer holder with double o-ring. After fabrication of the devices, ProTEK B3 primer was spin-coated on the front side at 1500 rpm for 30 s with an acceleration of 10000 RPM/s. Then the wafers were baked on a hotplate at 140˚C for 120 s followed by 205˚C for 5 minutes in a convection heating oven. Following the step, the ProTEK B3 protective coating was spin-coated on the front side at 1500 rpm for 60 s with an acceleration of 10000 RPM/s. The wafers were then baked on a hotplate at 140˚C for 120 s and at 205˚C for 30 minutes in a convection heating oven. For further protection, the wafer was placed in a holder with double o-ring. After chemical thinning from rear side (Fig. 1d), the front ProTEK protection mask was removed by repeatedly rinsing it in fresh acetone and methanol for 4 times until the solution becomes clear. Then, the wafer-scale transfer method **(**Figs. 1e-1l) followed to obtain the UTCs on polyimide. Before transferring the samples, the central section of polyimide was removed to expose the back contacts. After transferring to polyimide, copper tape (50 μm thick) was used as back contact of devices. The tape also serves as the thermal dissipation layer, which is needed for high performance computing. Instead of using polyimide, the hot lamination of PVC was used to encapsulate the MOSFETs. To gain access to contact pads the openings were cut on the top of the PVC using Silhouette cutter before laminating the devices.

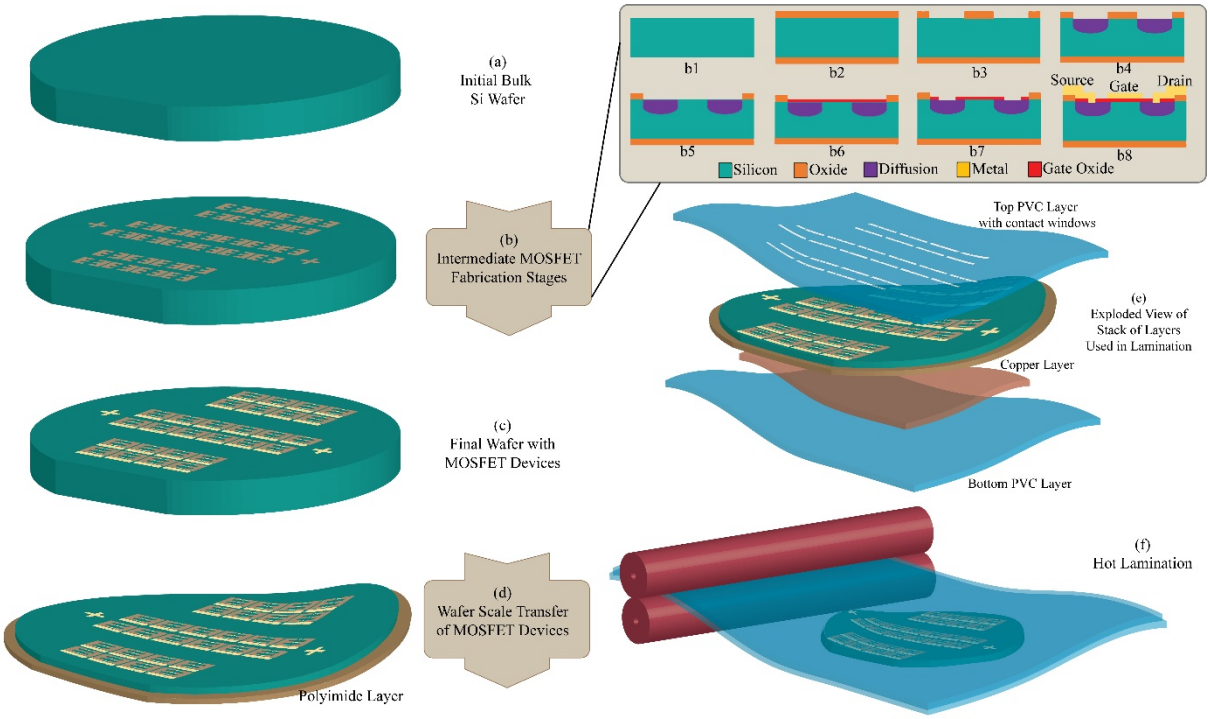


**Figure 2.** Illustration of wafer-scale MOSFET fabrication, thinning and packaging

The proposed methodology for wafer-scale transfer of UTCs has many advantages including compatibility with conventional CMOS process for mass-production. Besides this the proposed method allows easy integration of UTCs on foil because steps such as metallization (e.g. for extended contact pads) can be easily performed on the wafer itself i.e. before releasing the UTCs. Further it is possible to cut and paste the UTCs on any substrate to enable products with heterogeneous integrated systems-on-foil[15, 33, 35]. The easy handling UTCs and thin wafers can increase the production yield. The methodology does not require sophisticated instruments such as precise pick and place tools.

### 3. Results and Discussion

The above devices were studied in detail to gain insight into the effectiveness of proposed methodology. We first investigated the effect of thinning on surface morphology and optical properties, which are common to all samples (**Table 2**). High performance circuits for various application requires majorly resistors, capacitors, MOSFETs, sometimes inductors and other circuit elements. To study the effect of tensile and compressive bending on response of such

circuit, we studied electrical characteristics of resistive structures, MOS capacitor and n-MOSFET. Further, many standard abstract models depending on the regions of operation consider MOSFET device as comprising of a combination of voltage controlled resistive (channel region) and capacitive components along with other parasitics, this step-wise study gives a better insight on bending induced deviations in their response[36]. Various samples used in this study are summarised in **Table 2** with their dimensions and key-findings.

### 3.1. Surface Morphology

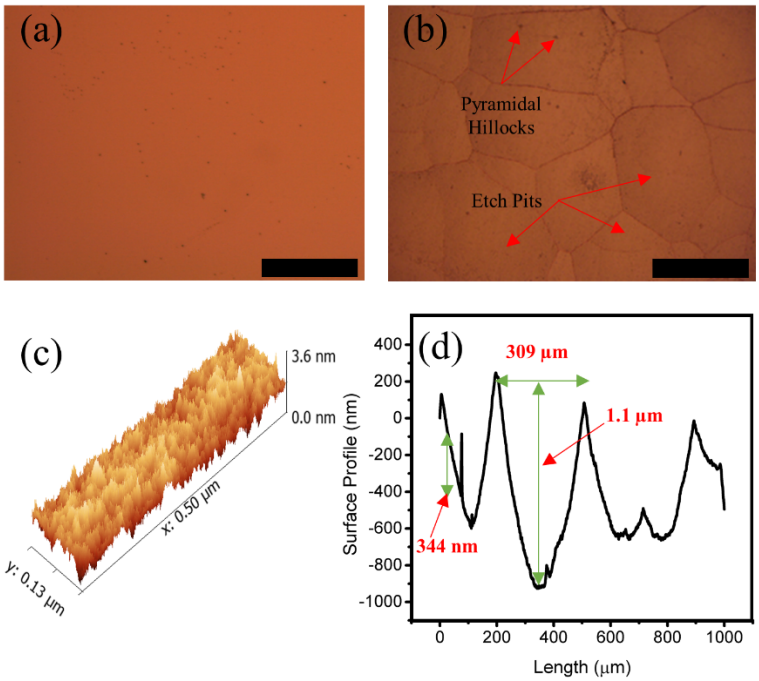


**Figure 3**. Optical microscopic images of a) front and (Scale: 400 µm) b) rear surface of the thinned Si (Scale: 400 µm) showing etch pits and pyramidal hillocks. c) Atomic Force Microscopy (AFM) scan of the front surface of the thinned Si showing a root-mean-square (RMS) surface roughness of 0.392 nm d) Surface profile of rear side showing etch pits (~1.1 µm deep, ~309 µm wide), pyramidal hillocks (~344 nm high) and Gaussian Filtered RMS surface roughness of 132 nm.

During the anisotropic wet etching, it is possible to have pyramid shape hillocks on the etched surface which leads to localized stress and can adversely affect the strength of the chip[37]. While hillocks could be reduced by adding IPA to etchant, the etch pits seem to be inherent to process.

Such morphological features influence the fracture strength of Si and therefore careful selection of etchant is needed to have highest possible fracture strength along with smooth etched surface[37]. For this reason, we used IPA/TMAH solution which is widely reported to improve the surface smoothness by increasing wettability of the TMAH etchant and decreases the formation of the hydrogen bubbles[38]. We studied the microscopic surface morphology of both sides of the wafer as can be seen from optical and AFM scan images in **Figure. 3(a)** and **Figure. 3(c),** the front surface is smooth with RMS surface roughness up to ~0.392 nm. However, some etch-pits and pyramidal hillocks appear on the rear surface of the sample as shown in the optical microscopic image (**Figure. 3(b))** and surface profilometer scan (**Figure. 3(d))**. Careful examination of the etched surface reveals that the surface is almost built up with circular etch pits which are ~1.1 μm deep and ~309 μm wide.

### 3.2. Optical Analysis and UV-Visible-NIR spectroscopy

Si starts to become optically transparent with decrease in the thickness, starting in the red region and progressing towards blue region as the wafer becomes thinner. This is owing to varying absorption coefficients of Si at different wavelengths. The Fresnel equation and Beer-Lambert law could be used to estimate the percentages of reflected and absorbed lights for Si thickness (>10 μm) which is not of the order of the wavelengths of the light spectrum (300 nm to 1100 nm), where interference effects are negligible. **Supplementary Section S1** gives these equations.

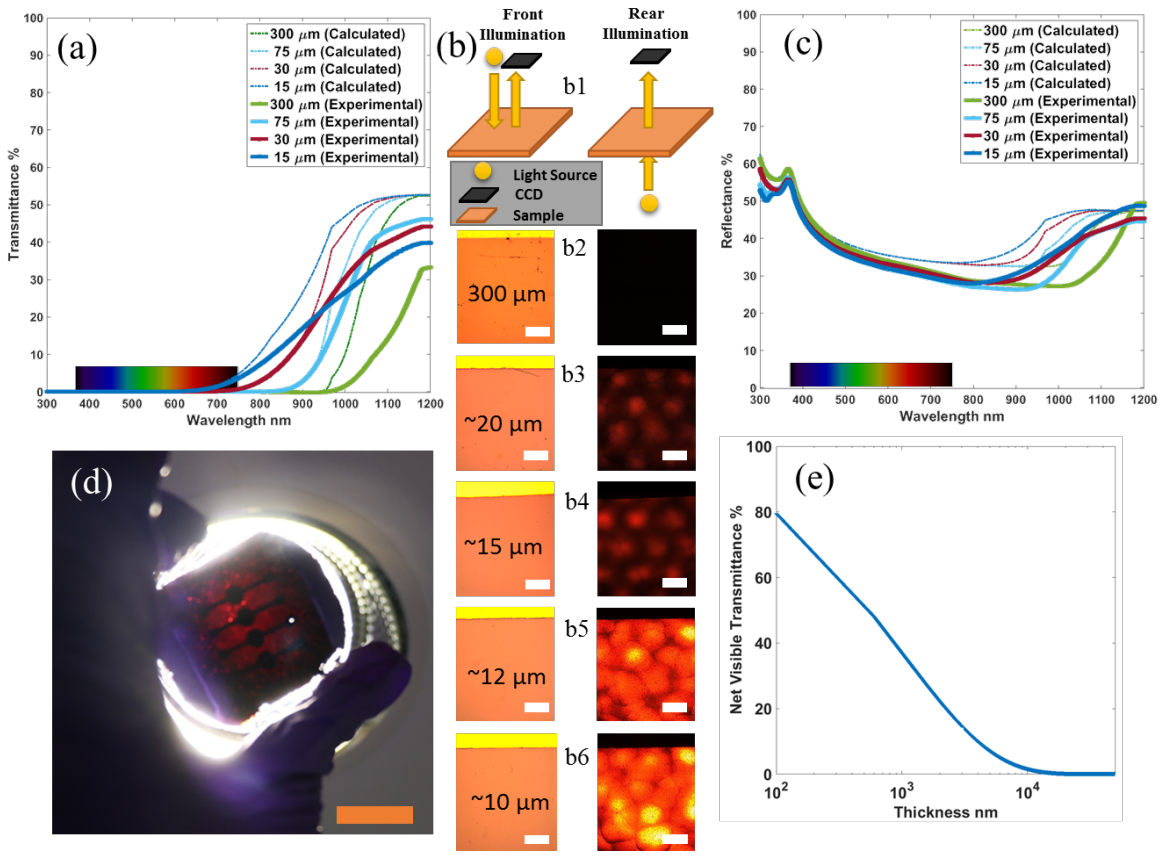


**Figure 4.** UV-Visible-NIR a) transmittance and c) reflectance spectrum compared to the calculated spectrum for various thicknesses of Si chips b) Schematic b1) and Optical microscopic images of samples b2-b6) of different thickness imaged from front-side under front-side illumination and rear-side illumination (Scales: 300 μm). d) Thin silicon MOS capacitor structure transmitting red light under a white led light illumination (Scale: 2 cm). e) Net visible transmittance Versus Thickness of wafer.

**Figure. 4(a)** and **Figure. 4(c)** shows the net spectral transmittance and spectral reflectance, respectively of the ultrathin silicon samples namely UVN1, UVN2, UVN3 and UVN4, corresponding to thicknesses 15 μm, 30 μm, 75 μm and 300 μm, as given in **Table. 2** (UVN stands for sample used for UV-Visible-Near-Infrared spectroscopic studies). The UV-Visible-NIR spectroscopic investigation was carried out using Shimadzu UV2600 spectrophotometer with a 60mm integrating sphere. The dashed thin lines in the figures correspond to the

calculated spectral transmittance and spectral reflectance. Overall, silicon's absorption coefficient becomes lower towards red and NIR region causing an observable increase in both transmittance and reflectance (contribution from front and rear side) towards the red end of the spectrum. Since the calculations consider only specular reflectance there is a difference observed between the calculated and measured spectrum especially in the NIR and the red region. Out of the light passing through the silicon, blue and green region gets absorbed completely within 10 μm. Beyond that the absorptance decreases and reaches minimum at ~1150 nm wavelength which corresponds to the bandgap of the silicon. The photons passing through the silicon wafer gets reflected from rear end. Since the starting bulk wafer (UVN4 ~300 μm) had a saw cut and alkaline etched rear side textures (optical microscopic image in **supplementary section S2**) it results in higher scattering of the red and IR photons causing them to absorb in the wafer. As the wafer is etched for long time in 25% TMAH with 10% IPA the small textures get smoothened out and shallow etch pits appear as shown in **Figure. 3b**. This along with thinning results in higher reflectance and transmittance in the infrared end of spectrum. The normalized net transmittance of the four samples UVN1 (~15 μm), UVN2 (~30 μm), UVN3 (~75 μm) and UVN4 (~300 μm) were 8.694%, 8.380%, 6.09% and 0.927% respectively. In the visible region UVN4 and UVN3 didn't have any observable transmittance. UVN2 and UVN1 had very low transmittances of 0.011% and 0.170% respectively. The effect is well observed in **Figure. 4(b2-b6)** where Si wafers of various thicknesses at various stages of thinning were illuminated as schematically shown in **Figure. 4(b1).** The illumination was carried out both from front side (reflection) as well as the rear side (transmission) while the image was captured always from the front side in an optical microscope**.** The top strip appearing as yellow in the top illumination and black in the bottom illumination of all the images in **Figure. 4(b2-b6)**) correspond to the metal used as electrode of the capacitive structure. In the sample with thickness ~300 μm, complete opaqueness is observed across the visible spectrum. However, when the thickness reaches sub-20 μm range, even though the sample looks similar

in the front illumination transparency in red region starts being visible **Figure. 4(b3-b6).** The etch pit boundaries are also visible in the rear illumination. **Figure. 4(d)** shows the thinned MOSCAP wafer corresponding to **Figure. 6(a)** (electrical characteristics discussed later in this section) under rear illumination by a white LED light. One possible application of this behaviour could be to decide the etch stop time. Since in wet etching, the etch time plays a crucial rule and very hard to control, a red-light source could be placed at one end of etching setup and the transmittance can then be observed from other side. When the transmittance crosses the limit, which corresponds to particular thickness, etching can be stopped. This will assist in large scale manufacturing of ultrathin chips. For application where higher absorptance is required, such as flexible silicon based solar cells, the optical path length in thin silicon can be improved by using special optical trapping techniques such as Lambertian trapping[39], texturing, antireflection coatings[40]. **Figure. 4(e)** shows normalized weighted transmittance in the visible region for various thicknesses. 80% weighted visible transmittance can be achieved for Si close to 100nm thick. Such thin Si could find application to realize semi-transparent or transparent electronics. Realizing this is possible using SOI technology where the oxide layer underneath could act as a supporting transparent layer for thin Si along with serving as an etch stop layer.

### 3.3. Effect of Bending on the devices

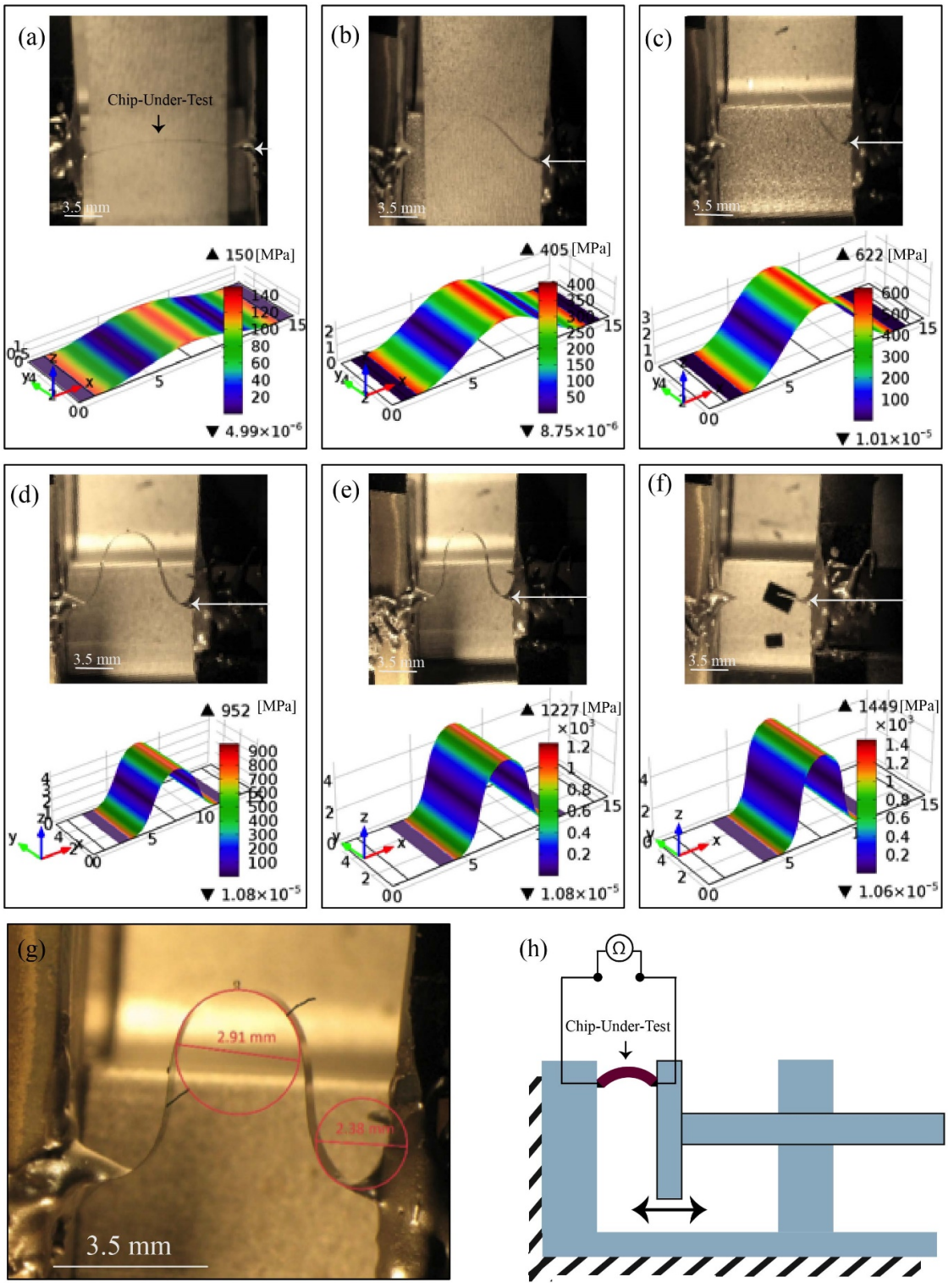


**Figure 5**. a-f) Bending of bare Si chips anchored on both sides by silver paste together with COMSOL simulation of Von Mises Stress. g) enlarged image of Fig. 2(e) showing the diameter of curvature of the film implying a $R_C = 1.19$ mm just before breakage (with angle correction). h) Schematic of electro-mechanical bend test setup.

It is important to examine the limits of bending and understand the stress-strain in single and multilayer electronic structures to ensure reliable operation of UTCs[15, 41]. Therefore, the UTC samples were investigated by: (a) semi-analytical approach; (b) experimental bending analysis, and (c) finite element analysis in COMSOL. For bending analysis, we tested three types of samples i.e. RBC1, RBC2 and RBC3, as described in **Table 2**.

The samples were placed on the clamps connected to a micrometer positioning set up as illustrated in **Figure. 5(h)**. The sample bends as the movable end advances towards the fixed end during which images were recorded at various stages of bending as shown in **Figure. 5(a-f)** (for sample RBC2). Similar figures for RBC1 and RBC3 are provided in the **Supplementary Section S3**. These images were also used to determine the various radius of curvature, $R_C$ by estimating the distance per pixel from the two ends of the jig and the number of pixels in the diameter formed by the circle fitting into the curved membrane with angle correction. Since the bending was carried out by anchoring the UTC between the moving and fixed jig, the top centre of the chip is under tensile stress while the top left and right edges are in compressive stress. Bottom centre of the chip is in compressive stress while the bottom left and right edges are in tensile stress. The stress varies along the thickness as well as from centre to periphery as observed in the COMSOL simulation results in **Figure. 5** Von Mises Stress. The distance between the two ends of the jig versus 1/Radius of Curvature at the centre is given in **Figure. S4(a**) in **Supplementary Section S4**. The breaking radius of curvature, $R_{BC}$ is the $R_C$ just before the ultrathin chip breaks. The experimental and theoretical values of $R_{BC}$ are summarized in **Table 2** and its derivation is given in the **Supplementary Section S5**. The equation and the parameters used for COMSOL simulation are given in **Supplementary Section S6**. It may be noted that the breaking radius decreases or the structures becomes less conformable with multiple layers of materials on UTCs especially when the UTC position is shifted away from the neutral plane instead of a symmetric condition. For example, theoretical value of $R_{BC}$ for RBC3 is ~1.475 mm, whereas the same for MOSCAP and MOSFET is ~18.897 mm.

During the bending, we also measured the electrical resistance of the membrane (RBC2 and RBC3) using the contacts at the two ends. With UTCs bending, the top p-side (i.e. doped side) experiences a tensile strain while bottom n-side experienced a compressive strain. While the tensile strain increases the resistance of p-side, compressive strain increases the value of n-side, and since these two resistors can be in parallel, we may see an increase in combined resistance value. This results in an overall increase in the resistance of UTCs, which is mainly attributed to the piezo-resistivity. For bare Si chip (RBC2), the base resistance (i.e. corresponding to the initial zero bending state) was found to be 17.27 kΩ and a maximum increase of 3.8% was observed just before the breaking radius of curvature (**Figure. S4-(b)**). In case of polyimide (PI)/Si/PI (RBC3), the base resistance was 6.21 kΩ with a maximum percentage increase of 1.2%. This neglects the region closer to the breaking radius of curvature where the resistance went up to >14.2 kΩ as can be seen from **Figure. S4-(c)**. The sudden increase in resistance could be attributed to microcracks possibly developed at the contacts but the polyimide keeping the structure together.

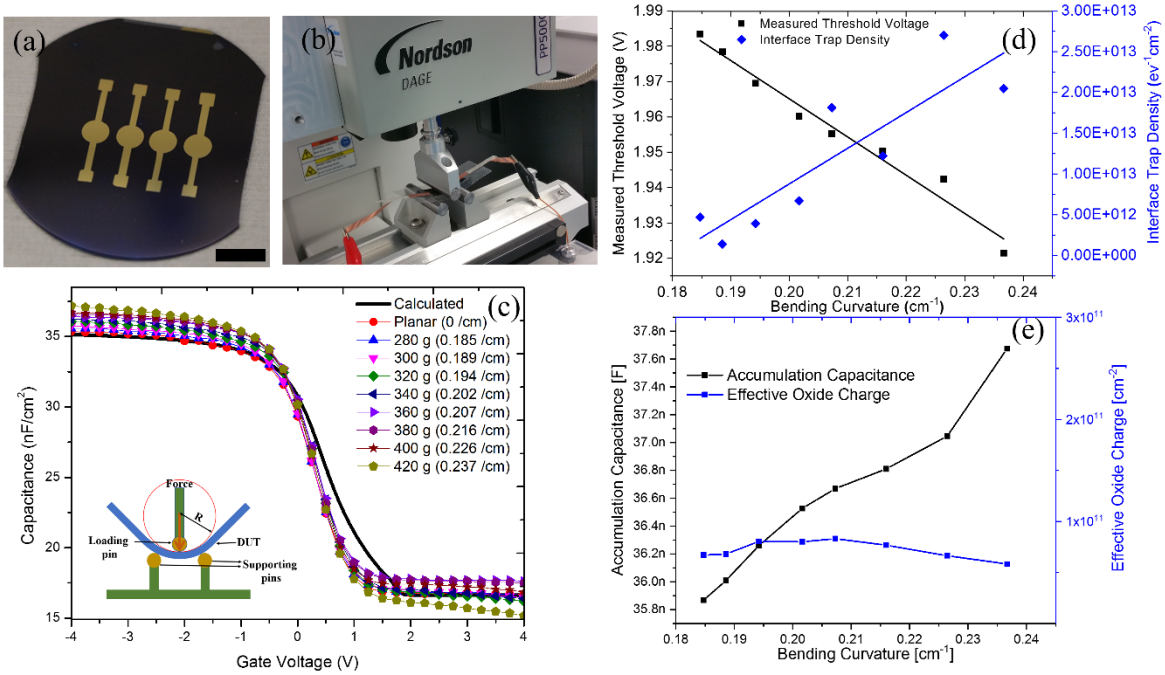


**Figure 6.** a) Image of fabricated MOSCAPs (scale: 1 cm). b) Device Under Test (DUT) under 3-point bending setup. c) C-V characteristics under ideal and various bending conditions. d)

Bending curvature Vs threshold voltage and interface trap density. e) Bending curvature Vs accumulation capacitance and effective oxide charge

MOS capacitor is an essential part of a MOSFET. So, to study the effect of bending on MOSFET, it is necessary to study how various parameters change during the bending of MOS capacitor. The MOSCAP was evaluated for bending by using a Nordson Dage 3-point bending set up (**Figure. 6(b)**). The samples were encapsulated in poly(vinyl chloride) (PVC) sheets using hot lamination method and then various loading forces and corresponding displacements were measured. The C-V measurements of the MOSCAP device under planar and various bending conditions (**Figure. 6(c)**) were made with a semiconductor parameter analyser at 1MHz frequency. The C-V sweep was carried out with DC voltage from -4 to 4 Volts superimposed with a 50 mV AC voltage. Change in the CV characteristics was observed with bending and up to 5% increase in capacitance was measured at bending radius of 42 mm. The bending radius of curvature was calculated from the vertical displacement assuming the membrane width as arc length and displacement as chord of a circle. The ideal CV characteristics calculated with MATLAB code with given doping and oxide thickness corresponding to accumulation capacitance is also shown in **Figure. 6(c)** and derivation of ideal CV is provided in supplementary material (**Section S7**). The measured CV characteristics differ from the calculated value due to the presence of various charges in the oxide (namely, fixed oxide charges, mobile ionic charges, interface trapped charges), work function of the metal, interface trap density as well as the effect of bending on doping and other parameters. It may be noted from **Figure. 6(d)** that the interface trap density increases and the $V_{th}$ decreases as the bending curvature increases. In addition, an increase in accumulation capacitance value upon increasing tensile strain was observed and plotted in **Figure. 6(e).** Also, it is worthy to note that the effective oxide charge value remained almost constant during bending. **Supplementary figure S9 shows the** Flatband Capacitance and Flatband Voltage Vs Bending Curvature of

MOSCAP. The variation in threshold voltage upon bending, can change the operating point of device and so proper compensation circuit might be needed. Various device and interface parameters extracted by comparing the measured and ideal CV characteristics are summarized in **Table 3**.

**Table 3. Various MOSCAP parameters calculated from C-V characteristics obtained from planar condition**

| MOSCAP Parameters in planar condition | Value |
|---|---|
| Threshold voltage | 1.99319 V |
| Effective oxide charge | $6.88 \times 10^{10}$ /cm$^2$ |
| Interface trap density | $8.65 \times 10^{11}$ /cm$^2$-eV |
| Depletion width | 327 nm |
| Flatband capacitance | 31.1 nF |
| Flatband voltage | -0.189 V |
| Accumulation capacitance | 35.6 nF/cm$^2$ |

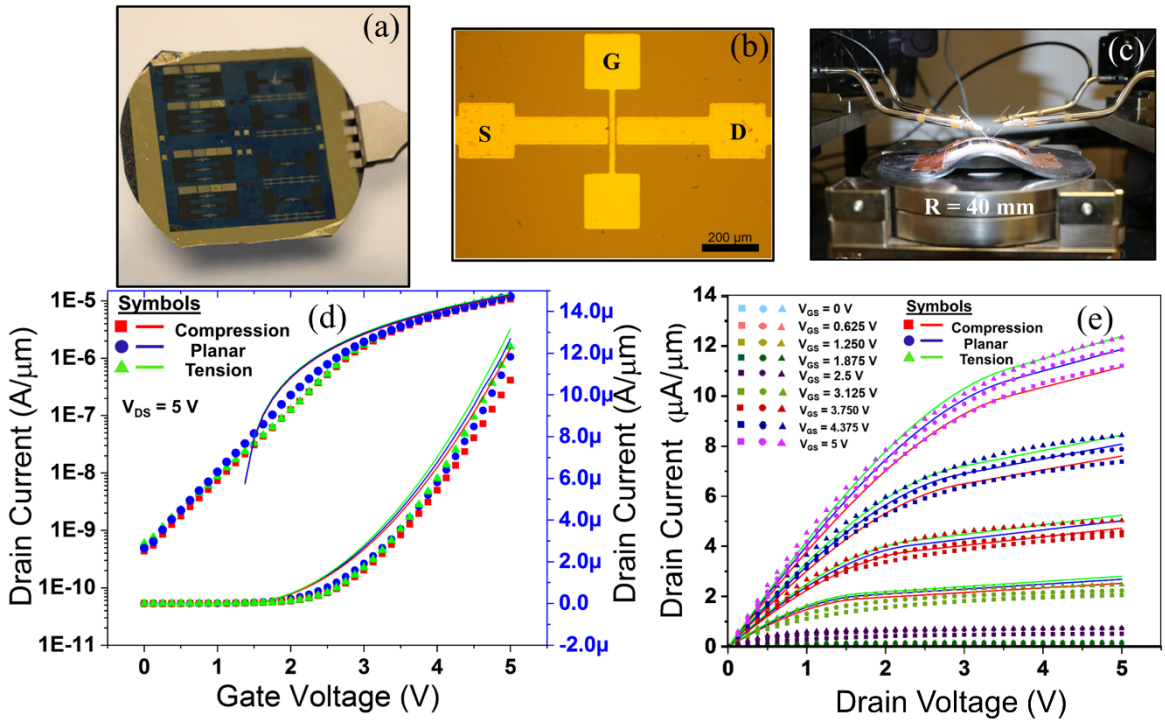


**Figure 7.** a) Si wafer with MOSFETs. b) Optical image of single MOSFET (W = 100 µm, L=10 µm). c) Arrangement for electrical characterisation under bending conditions. The wafer with MOSFETs placed on the curved surface of 3D printed structures. d) Transfer characteristics of MOSFET [experimental (dots) Vs simulation (line)] under planar (blue line), compressive (red line) and tensile (green line) bending conditions. e) Output characteristics of MOSFET [experimental (dots) Vs simulation (line)] under planar (blue line), compressive (red line) and tensile (green line) bending conditions.

The fabricated MOSFET devices on wafer-scale are shown in **Figure. 7(a).** The microscopic image of a single MOSFET is shown in **Figure. 7(b).** After thinning and transfer printing as described before, the MOSFET devices were tested under various bending conditions. To observe the effect of bending stress, the laminated thinned wafer was placed on 3D printed convex and concave structures (R = 40 mm) as shown in **Figure. 7(c)**. In convex bending, the devices come under tensile stress whereas they experience compressive stress in the case of concave bending. The strain generated due to mechanical bending is known to affect the band structure of material[42]. In planar condition, the conduction band minimum of Si consists of six degenerate $\Delta_6$ valleys which splits into two groups $\Delta_4$ and $\Delta_2$ under strain. Under tensile strain, the energy of $\Delta_4$ gets lowered down with respect to $\Delta_2$ and vice-versa for compressive strain. Similarly, tensile strain decreases the energy level of all three-valence bands and compressive strain increases their energy level. The effective mass of carrier is obtained using E-k model either at the bottom of conduction band or at the top of valence band. This splitting and lowering of bands in devices under tensile stresses decreases the effective mass and opposite happens in the case of compressive strain. Due to change in the effective mass, the charge surface carrier mobility (μ) changes. In previous works, we formulated analytical equations relating the stress with the mobility and drain current[41, 43].

$$\mu_{(\text{stress})} = \mu_o\left(1 \pm \Pi_\mu \sigma_\mu\right) \tag{5}$$

$$I_{D(\text{stress})} = I_{D_0}\left(1 \pm \Pi_{I_D} \sigma_{I_D}\right) \tag{6}$$

where $\mu_0$, $I_{D0}$, $\mu_{stress}$ and $I_{Dstress}$ are mobility and drain current under normal and stressed conditions respectively. The piezo-resistive coefficients $\Pi_\mu$ and $\Pi_{ID}$ accounts for sensitivity towards stress and $\sigma$ is magnitude of stress[36b]. In n-MOSFET, the channel is n-type where the resistance decreases and gate oxide capacitance increases with tensile bending. This means the tensile strain leads to overall increase in the current and opposite happens for compressive strain. This is indicated by the transfer and output characteristics of transistor in **Figure. 7(d)** and

**Figure. 7(e)** respectively. These characteristics were obtained under different bending conditions. Various parameters extracted from the electrical characterisation of the MOSFET under planar and bending conditions are summarized in **Table 4**. The effective surface mobility $\mu_{eff}$ was calculated by the equation:

$$\mu_{eff} = \frac{L}{W}\frac{g_d}{C_{ox}(V_{GS}-V_{th})} \quad (7)$$

Where L and W are the length and width of the MOSFET, $g_d$ is the drain conductance, $C_{ox}$ is the oxide capacitance and $V_{th}$ is the threshold voltage. The threshold voltage (extracted from linear extrapolation method[44]) under tensile bending, planar and compressive bending conditions are 1.305, 1.425 and 1.55 V, respectively. The drain conductance is given by the equation:

$$g_d = \frac{\partial I_D}{\partial V_{DS}}|V_{GS} = Constant \quad (8)$$

The drain conductances at tensile, planar and compressive conditions were estimated from the $V_{DS}$-$I_D$ characteristics by numerically differentiating the drain current with reference to the drain-source voltage and their values were 4.94, 4.58 and 4.06 µS/µm respectively. The maximum transconductance of the n-MOSFET under planar and bending conditions were calculated as per the equation by numerically differentiating the values in Matlab:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}|V_{DS} = Constant \quad (9)$$

The estimated effective surface mobility for the three conditions were 384, 350 and 333 *$cm^2$/V-s,* respectively.

**Table 4. Various parameters related to MOSFET characteristics**

| Parameters | Tensile Strain | Planar | Compressive Strain |
|---|---|---|---|
| Bending Radius of Curvature $R_C$ | 40 mm (Convex) | - | 40 mm (Concave) |
| Effective Mobility (Experimental) $\mu_{eff}$ | *384 $cm^2$/V-s* | *350 $cm^2$/V-s* | 333 *$cm^2$/V-s* |
| Saturation Mobility (Experimental) $\mu_{sat}$ | 355 *$cm^2$/V-s* | 341 *$cm^2$/V-s* | 320 *$cm^2$/V-s* |
| Saturation Mobility (Semi-empirical) $\mu_{sat\text{-}Cal}$ | *353 $cm^2$/V-s* | *341 $cm^2$/V-s (Ref.)* | 327 *$cm^2$/V-s* |
| Threshold voltage ($V_{th}$) | *1.305 V* | *1.425 V* | 1.55 V |
| Channel-length Modulation Factor (λ) | *0.094* | *0.115* | 0.122 |
| Saturation Current ($I_{D\text{-}sat}$) at $V_{DS}$=5 and $V_{GS}$=5V | 12.3 µA/µm | 11.8 µA/µm | 10.7 µA/µm |
| Drain Conductance ($g_d$) | 4.94 µS/µm | 4.58 µS/µm | 4.06 µS/µm |
| $I_{ON}/I_{OFF}$ | 4.32 decades ($2.08 \times 10^4$) | 4.38 decades ($2.42 \times 10^4$) | 4.39 decades ($2.46 \times 10^4$) |
| SS | 1.06 V/decade | 0.98 V/decade | 1.04 V/decade |
| Transconductance ($g_m$) | 6.67 µS/µm | 6.62 µS/µm | 6.21 µS/µm |
| Gate Delay | 0.23 ns | 0.27 ns | 0.3 ns |

The saturation mobility ($\mu_{sat}$) obtained from output characteristics under planar condition is 341 *$cm^2$/V-s*. However, with convex and concave bending, the mobility (with same biasing conditions) was found to be 355 *$cm^2$/V-s* and 320 *$cm^2$/V-s* respectively. Using Equation. 5 and Equation. 6, the semi-empirically (in relation to planar saturation mobility) estimated value of mobilities under tensile (convex) and compressive (concave) bending are 353 *$cm^2$/V-s* and 327 *$cm^2$/V-s* (Calculations in supplementary **section S8**). Thus, semi-empirical values closely match and deviate only by 0.5% and 2.5% from the experimentally obtained mobility values.

The change in current level can be primarily attributed to change in oxide capacitance, interface effects and mobility. Since, current is directly proportional to both capacitance and mobility, for small change, it can be written as:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta C_{ox}}{C_{ox}} + \frac{\Delta \mu}{\mu} \tag{7}$$

At R = 40 mm, the theoretical change in mobility and capacitance are around 3.82% and 5% respectively, which lead to about 8% change in the current. This also matches with experimental measurements, which show a maximum of ~10% change in the current. The saturation current (at $V_{DS}$=*5V* and $V_{GS}$=5V) were 12.3, 11.8, 10.7 μA/μm for tensile, planar and compressive conditions respectively. The on-to-off current ratios for the three cases were 4.32, 4.38 and 4.39 decades. Subthreshold slope (SS) was estimated from the logarithmic transfer characteristics at subthreshold regime by numerical differentiation and is given by the equation:

$$SS = \frac{1}{\partial \log(I_D)/\partial V_{GS}} \tag{8}$$

The subthreshold slope for tensile, planar and compressive conditions were 1.06, 0.98 and 1.04 V/decade. The SS values are higher because the device was a planar, long channel MOSFET, with ~100 nm $SiO_2$ as dielectric. By realizing, advanced FET structures such as FinFET and by using High-K dielectric better subthreshold voltage can be achieved[18b]. The approximate gate

delay for a typical CMOS application assuming a fanout ($f_n$) of 2 and symmetric balanced CMOS (i.e. $\mu_{eff}$, L and W of n-MOS and p-MOSFET) was indirectly calculated from the below equation[36c]:

$$\tau_{GD} = \frac{12\, f_n}{\mu_{eff}} L_{Min}^2 \frac{V_{DD}}{(V_{DD}-V_{th})^2} \quad (10)$$

The calculated gate delays were 0.23, 0.27 and 0.3 ns for tensile, planar and compressive conditions which implies ~3 GHz operation with a variation of ~11 to 15%.

In order to evaluate the effect of cyclic bending on device performance, we characterised the MOSFET in planar condition after every 10 cycles of compressive and tensile bending over 3D printed zig of $R_C$ 80 mm. A total of 100 bending cycles were carried out. Gate leakage current density ($J_G$) characteristics were also obtained during initial planar condition and after 50$^{th}$ and 100$^{th}$ cycle. The plots of MOSFET transfer characteristics and leakage current densities are shown in Figure 8(a) and Figure 8(b) respectively. Statistically the device performance remains unaffected even after 100 bending cycles with an inter quartile range variation of less than 1.1% in $I_{DSAT}$ and negligible variation in the leakage current density when the gate voltage is positive. In order to evaluate the device-to-device variability four MOSFETs were characterized at various locations and the results are shown in in Figure 8(c). The device characteristics of three out of four devices were uniform with a variation of 3% in the $I_{DSAT}$.

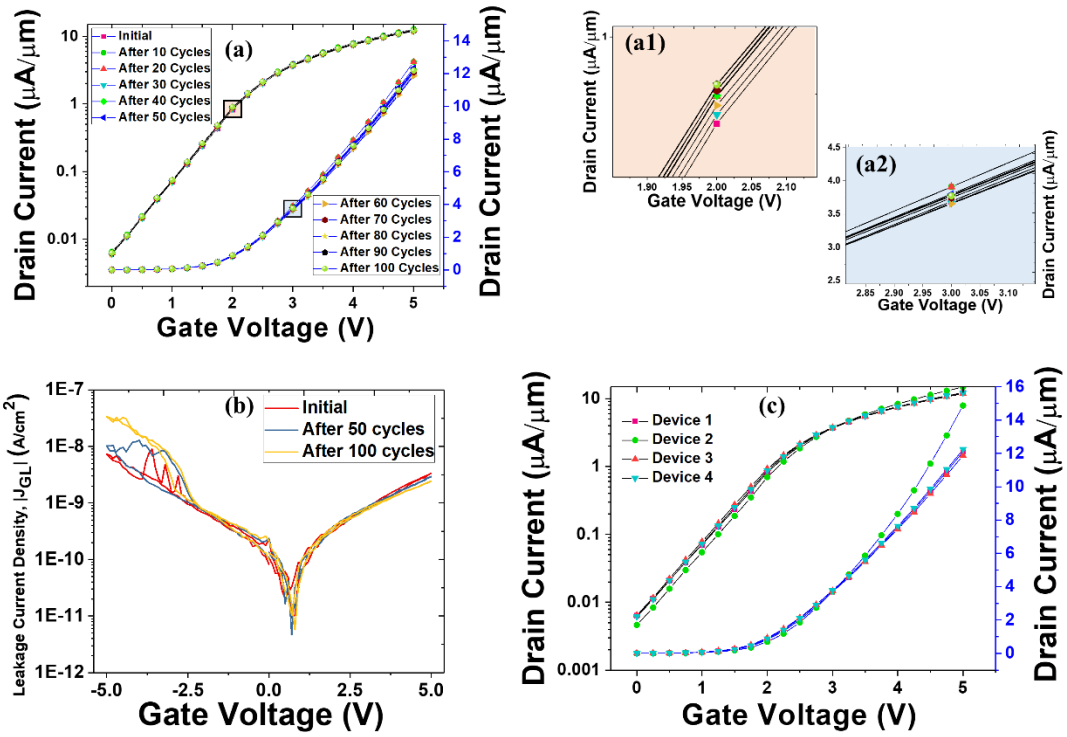


Figure 8. a) Transfer characteristic of MOSFET under cyclic bending test. b) Leakage current density of MOSFET at Initial condition, mid and end of cyclic bending test. c) Device-to-device variation in transfer characteristics for four MOSFETs.

The changes in device response with bending has a bearing on the performance of circuits and evaluation of devices response under various bending conditions will help electronic designers to consider such variations in their design – either to negate such effects or to take advantage (for example, improving device performance by introducing stresses or using stress map to predict the shape of ultra-thin chip or the surface on which the chips are integrated). Moreover, by further thinning (for e.g. using Chemical Mechanical Polishing) and optimal packaging in material of less young's modulus and in the neutral plane the stress variation can be reduced significantly.

## 4. Conclusion

The high-performance requirement for various flexible electronics applications can be met with Si based electronics, if ways can be found to overcome the rigidness and brittle nature of Si. In

this direction, the novel approach for wafer-scale transfer of UTCs on flexible substrates presented in this paper is promising. The methodology has been used to obtain Si chips (~15 μm thick) with various devices including resistors, MOSCAP and MOSFETs on polyimide substrate and they have been analysed for critical bending, surface micro-morphology and the change in optical properties. The optical study carried out through UV-Visible-NIR, shows that as the thickness of Si decreases, the transparency increases in the red region. This property could be used to control the etching or for new applications such as detectors where certain degree of transparency is needed close to red region. Chemical thinning of bulk silicon chips may not be an effective strategy for achieving transparent silicon due to the etch pit and hillocks formation. For this, a combination of anisotropic etching (to realize ~15 μm silicon) and subsequent chemical mechanical polishing could be helpful. The changes in the response of MOSFETs during electro-mechanical characterisation closely match with the theoretical calculations, which allows modelling the behaviour of these devices with conventional CAD tools. This will open new opportunity for designing circuits on flexible substrate and evaluation of their performance.

As for the future, several directions are interesting for this technology, either including integration of driver chips into flexible displays, as separate flexible packages, or directly integrated into the display substrates.

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